

C51004-1.3

Operating Conditions

Cyclone devices are offered in both commercial, industrial, and extended-temperature grades. However, industrial-grade and extended-temperature-grade devices may have limited speed-grade availability.

Tables 4–1 through 4–16 provide information on absolute maximum ratings, recommended operating conditions, DC operating conditions, and capacitance for Cyclone devices.

Table 4–1. Cyclone Device Absolute Maximum Ratings Notes (1), (2)

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCINT}	Supply voltage	With respect to ground (3)	-0.5	2.4	V
V_{CCIO}			-0.5	4.6	V
V_I	DC input voltage		-0.5	4.6	V
I_{OUT}	DC output current, per pin		-25	25	mA
T_{STG}	Storage temperature	No bias	-65	150	°C
T_{AMB}	Ambient temperature	Under bias	-65	135	°C
T_J	Junction temperature	BGA packages under bias		135	°C

Table 4–2. Cyclone Device Recommended Operating Conditions (Part 1 of 2)

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCINT}	Supply voltage for internal logic and input buffers	(4)	1.425	1.575	V
V_{CCIO}	Supply voltage for output buffers, 3.3-V operation	(4)	3.00	3.60	V
	Supply voltage for output buffers, 2.5-V operation	(4)	2.375	2.625	V
	Supply voltage for output buffers, 1.8-V operation	(4)	1.71	1.89	V
	Supply voltage for output buffers, 1.5-V operation	(4)	1.4	1.6	V
V_I	Input voltage	(3), (5)	-0.5	4.1	V

Table 4–2. Cyclone Device Recommended Operating Conditions (Part 2 of 2)

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_O	Output voltage		0	V_{CCIO}	V
T_J	Operating junction temperature	For commercial use	0	85	°C
		For industrial use	-40	100	°C
		For extended-temperature use	-40	125	°C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

Table 4–3. Cyclone Device DC Operating Conditions Note (6)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
I_I	Input pin leakage current	$V_I = V_{CCIO_{max}}$ to 0 V (8)	-10		10	µA
I_{OZ}	Tri-stated I/O pin leakage current	$V_O = V_{CCIO_{max}}$ to 0 V (8)	-10		10	µA
I_{CC0}	V_{CC} supply current (standby) (All M4K blocks in power-down mode) (7)	EP1C3		4		mA
		EP1C4		6		mA
		EP1C6		6		mA
		EP1C12		8		mA
		EP1C20		12		mA
R_{CONF}	Value of I/O pin pull-up resistor before and during configuration	$V_{CCIO} = 3.0$ V (9)	20		50	kΩ
		$V_{CCIO} = 2.375$ V (9)	30		80	kΩ
		$V_{CCIO} = 1.71$ V (9)	60		150	kΩ

Table 4–4. LVTTL Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO}	Output supply voltage		3.0	3.6	V
V_{IH}	High-level input voltage		1.7	4.1	V
V_{IL}	Low-level input voltage		-0.5	0.7	V
V_{OH}	High-level output voltage	$I_{OH} = -4$ to -24 mA (10)	2.4		V
V_{OL}	Low-level output voltage	$I_{OL} = 4$ to 24 mA (10)		0.45	V

Table 4–5. LVC MOS Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO}	Output supply voltage		3.0	3.6	V
V_{IH}	High-level input voltage		1.7	4.1	V
V_{IL}	Low-level input voltage		-0.5	0.7	V
V_{OH}	High-level output voltage	$V_{CCIO} = 3.0$, $I_{OH} = -0.1 \text{ mA}$	$V_{CCIO} - 0.2$		V
V_{OL}	Low-level output voltage	$V_{CCIO} = 3.0$, $I_{OL} = 0.1 \text{ mA}$		0.2	V

Table 4–6. 2.5-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO}	Output supply voltage		2.375	2.625	V
V_{IH}	High-level input voltage		1.7	4.1	V
V_{IL}	Low-level input voltage		-0.5	0.7	V
V_{OH}	High-level output voltage	$I_{OH} = -0.1 \text{ mA}$	2.1		V
		$I_{OH} = -1 \text{ mA}$	2.0		V
		$I_{OH} = -2 \text{ to } -16 \text{ mA}$ (10)	1.7		V
V_{OL}	Low-level output voltage	$I_{OL} = 0.1 \text{ mA}$		0.2	V
		$I_{OH} = 1 \text{ mA}$		0.4	V
		$I_{OH} = 2 \text{ to } 16 \text{ mA}$ (10)		0.7	V

Table 4–7. 1.8-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO}	Output supply voltage		1.65	1.95	V
V_{IH}	High-level input voltage		$0.65 \times V_{CCIO}$	2.25	V
V_{IL}	Low-level input voltage		-0.3	$0.35 \times V_{CCIO}$	V
V_{OH}	High-level output voltage	$I_{OH} = -2 \text{ to } -8 \text{ mA}$ (10)	$V_{CCIO} - 0.45$		V
V_{OL}	Low-level output voltage	$I_{OL} = 2 \text{ to } 8 \text{ mA}$ (10)		0.45	V

Table 4–8. 1.5-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO}	Output supply voltage		1.4	1.6	V
V_{IH}	High-level input voltage		$0.65 \times V_{CCIO}$	$V_{CCIO} + 0.3$	V
V_{IL}	Low-level input voltage		-0.3	$0.35 \times V_{CCIO}$	V
V_{OH}	High-level output voltage	$I_{OH} = -2 \text{ mA}$ (10)	$0.75 \times V_{CCIO}$		V
V_{OL}	Low-level output voltage	$I_{OL} = 2 \text{ mA}$ (10)		$0.25 \times V_{CCIO}$	V

Table 4–9. 2.5-V LVDS I/O Specifications Note (11)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	I/O supply voltage		2.375	2.5	2.625	V
V_{OD}	Differential output voltage	$R_L = 100 \Omega$	250		550	mV
ΔV_{OD}	Change in V_{OD} between high and low	$R_L = 100 \Omega$			50	mV
V_{OS}	Output offset voltage	$R_L = 100 \Omega$	1.125	1.25	1.375	V
ΔV_{OS}	Change in V_{OS} between high and low	$R_L = 100 \Omega$			50	mV
V_{TH}	Differential input threshold	$V_{CM} = 1.2 \text{ V}$	-100		100	mV
V_{IN}	Receiver input voltage range		0.0		2.4	V
R_L	Receiver differential input resistor		90	100	110	Ω

Table 4–10. 3.3-V PCI Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		3.0	3.3	3.6	V
V_{IH}	High-level input voltage		$0.5 \times V_{CCIO}$		$V_{CCIO} + 0.5$	V
V_{IL}	Low-level input voltage		-0.5		$0.3 \times V_{CCIO}$	V
V_{OH}	High-level output voltage	$I_{OUT} = -500 \mu\text{A}$	$0.9 \times V_{CCIO}$			V
V_{OL}	Low-level output voltage	$I_{OUT} = 1,500 \mu\text{A}$			$0.1 \times V_{CCIO}$	V

Table 4–11. SSTL-2 Class I Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		2.375	2.5	2.625	V
V_{TT}	Termination voltage		$V_{REF} - 0.04$	V_{REF}	$V_{REF} + 0.04$	V
V_{REF}	Reference voltage		1.15	1.25	1.35	V
V_{IH}	High-level input voltage		$V_{REF} + 0.18$		3.0	V
V_{IL}	Low-level input voltage		-0.3		$V_{REF} - 0.18$	V
V_{OH}	High-level output voltage	$I_{OH} = -8.1 \text{ mA}$ <i>(10)</i>	$V_{TT} + 0.57$			V
V_{OL}	Low-level output voltage	$I_{OL} = 8.1 \text{ mA}$ <i>(10)</i>			$V_{TT} - 0.57$	V

Table 4–12. SSTL-2 Class II Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		2.3	2.5	2.7	V
V_{TT}	Termination voltage		$V_{REF} - 0.04$	V_{REF}	$V_{REF} + 0.04$	V
V_{REF}	Reference voltage		1.15	1.25	1.35	V
V_{IH}	High-level input voltage		$V_{REF} + 0.18$		$V_{CCIO} + 0.3$	V
V_{IL}	Low-level input voltage		-0.3		$V_{REF} - 0.18$	V
V_{OH}	High-level output voltage	$I_{OH} = -16.4 \text{ mA}$ <i>(10)</i>	$V_{TT} + 0.76$			V
V_{OL}	Low-level output voltage	$I_{OL} = 16.4 \text{ mA}$ <i>(10)</i>			$V_{TT} - 0.76$	V

Table 4–13. SSTL-3 Class I Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		3.0	3.3	3.6	V
V_{TT}	Termination voltage		$V_{REF} - 0.05$	V_{REF}	$V_{REF} + 0.05$	V
V_{REF}	Reference voltage		1.3	1.5	1.7	V
V_{IH}	High-level input voltage		$V_{REF} + 0.2$		$V_{CCIO} + 0.3$	V
V_{IL}	Low-level input voltage		-0.3		$V_{REF} - 0.2$	V
V_{OH}	High-level output voltage	$I_{OH} = -8 \text{ mA}$ <i>(10)</i>	$V_{TT} + 0.6$			V
V_{OL}	Low-level output voltage	$I_{OL} = 8 \text{ mA}$ <i>(10)</i>			$V_{TT} - 0.6$	V

Table 4–14. SSTL-3 Class II Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		3.0	3.3	3.6	V
V_{TT}	Termination voltage		$V_{REF} - 0.05$	V_{REF}	$V_{REF} + 0.05$	V
V_{REF}	Reference voltage		1.3	1.5	1.7	V
V_{IH}	High-level input voltage		$V_{REF} + 0.2$		$V_{CCIO} + 0.3$	V
V_{IL}	Low-level input voltage		-0.3		$V_{REF} - 0.2$	V
V_{OH}	High-level output voltage	$I_{OH} = -16 \text{ mA}$ <i>(10)</i>	$V_{TT} + 0.8$			V
V_{OL}	Low-level output voltage	$I_{OL} = 16 \text{ mA}$ <i>(10)</i>			$V_{TT} - 0.8$	V

Table 4–15. Bus Hold Parameters

Parameter	Conditions	V_{CCIO} Level								Unit	
		1.5 V		1.8 V		2.5 V		3.3 V			
		Min	Max	Min	Max	Min	Max	Min	Max		
Low sustaining current	$V_{IN} > V_{IL}$ (maximum)			30		50		70		μA	
High sustaining current	$V_{IN} < V_{IH}$ (minimum)			-30		-50		-70		μA	
Low overdrive current	$0 \text{ V} < V_{IN} < V_{CCIO}$				200		300		500	μA	
High overdrive current	$0 \text{ V} < V_{IN} < V_{CCIO}$				-200		-300		-500	μA	

Table 4–16. Cyclone Device Capacitance Note (12)

Symbol	Parameter	Typical	Unit
C_{IO}	Input capacitance for user I/O pin	4.0	pF
C_{LVDS}	Input capacitance for dual-purpose LVDS/user I/O pin	4.7	pF
C_{VREF}	Input capacitance for dual-purpose V_{REF} /user I/O pin.	12.0	pF
C_{DPCLK}	Input capacitance for dual-purpose DPCLK/user I/O pin.	4.4	pF
C_{CLK}	Input capacitance for CLK pin.	4.7	pF

Notes to Tables 4–1 through 4–16:

- (1) See the *Operating Requirements for Altera Devices Data Sheet*.
- (2) Conditions beyond those listed in [Table 4–1](#) may cause permanent damage to a device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse affects on the device.
- (3) Minimum DC input is –0.5 V. During transitions, the inputs may undershoot to –0.5 V or overshoot to 4.6 V for input currents less than 100 mA and periods shorter than 20 ns.
- (4) Maximum V_{CC} rise time is 100 ms, and V_{CC} must rise monotonically.
- (5) All pins, including dedicated inputs, clock, I/O, and JTAG pins, may be driven before V_{CCINT} and V_{CCIO} are powered.
- (6) Typical values are for $T_A = 25^\circ C$, $V_{CCINT} = 1.5 V$, and $V_{CCIO} = 1.5 V, 1.8 V, 2.5 V$, and $3.3 V$.
- (7) V_1 = ground, no load, no toggling inputs.
- (8) This value is specified for normal device operation. The value may vary during power-up. This applies for all V_{CCIO} settings (3.3, 2.5, 1.8, and 1.5 V).
- (9) Pin pull-up resistance values will lower if an external source drives the pin higher than V_{CCIO} .
- (10) Drive strength is programmable according to values in [Table 4–14](#).
- (11) The Cyclone LVDS interface requires a resistor network outside of the transmitter channels.
- (12) Capacitance is sample-tested only. Capacitance is measured using time-domain reflections (TDR). Measurement accuracy is within ± 0.5 pF.

Power Consumption

Designers can use the Altera web power calculator to estimate the device power.

Cyclone devices require a certain amount of power-up current to successfully power up because of the nature of the leading-edge process on which they are fabricated. [Table 4–17](#) shows the maximum power-up current required to power up a Cyclone device.

Table 4–17. Cyclone Power-Up Current (I_{CCINT}) Requirements

Device	Maximum Power-Up Current Requirement	Unit
EP1C3	300	mA
EP1C4 (1)	400	mA
EP1C6 (2)	500	mA
EP1C12	900	mA
EP1C20	1,200	mA

Notes to Table 4–17:

- (1) The EP1C4 maximum power-up current is an estimated specification and may change.
- (2) The EP1C6 maximum power-up current is for all EP1C6 devices except for those with lot codes listed in the *Cyclone FPGA Family Errata Sheet*.

Designers should select power supplies and regulators that can supply this amount of current when designing with Cyclone devices. This specification is for commercial operating conditions. Measurements were performed with an isolated Cyclone device on the board. Decoupling capacitors were not used in this measurement. To factor in the current for decoupling capacitors, sum up the current for each capacitor using the following equation:

$$I = C \cdot (dV/dt)$$

The exact amount of current that will be consumed varies according to the process, temperature, and power ramp rate. If the power supply or regulator can supply more current than required, the Cyclone device may consume more current than the maximum current specified in [Table 4–17](#). However, the device does not require any more current to successfully power up than what is listed in [Table 4–17](#).

The duration of the I_{CCINT} power-up requirement depends on the V_{CCINT} voltage supply rise time. The power-up current consumption drops when the V_{CCINT} supply reaches approximately 0.75 V. For example, if the V_{CCINT} rise time has a linear rise of 15 ms, the current consumption spike will drop by 7.5 ms.

Typically, the user-mode current during device operation is lower than the power-up current in [Table 4-17](#). Altera recommends using the Cyclone Power Calculator, available on the Altera web site, to estimate the user-mode I_{CCINT} consumption and then select power supplies or regulators based on the higher value.

Timing Model

The DirectDrive technology and MultiTrack interconnect ensure predictable performance, accurate simulation, and accurate timing analysis across all Cyclone device densities and speed grades. This section describes and specifies the performance, internal, external, and PLL timing specifications.

All specifications are representative of worst-case supply voltage and junction temperature conditions.

Preliminary & Final Timing

Timing models can have either preliminary or final status. The Quartus® II software issues an informational message during the design compilation if the timing models are preliminary. [Table 4-18](#) shows the status of the Cyclone device timing models.

Preliminary status means the timing model is subject to change. Initially, timing numbers are created using simulation results, process data, and other known parameters. These tests are used to make the preliminary numbers as close to the actual timing parameters as possible.

Final timing numbers are based on actual device operation and testing. These numbers reflect the actual performance of the device under worst-case voltage and junction temperature conditions.

Table 4–18. Cyclone Device Timing Model Status

Device	Preliminary	Final
EP1C3		✓
EP1C4	✓	
EP1C6		✓
EP1C12		✓
EP1C20		✓

Performance

The maximum internal logic array clock tree frequency is limited to the specifications shown in [Table 4–19](#).

Table 4–19. Clock Tree Maximum Performance Specification

Parameter	Definition	-6 Speed Grade			-7 Speed Grade			-8 Speed Grade			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Clock tree f_{MAX}	Maximum frequency that the clock tree can support for clocking registered logic			405			320			275	MHz

Table 4–20 shows the Cyclone device performance for some common designs. All performance values were obtained with the Quartus II software compilation of library of parameterized modules (LPM) functions or megafunctions. These performance values are based on EP1C6 devices in 144-pin TQFP packages.

Table 4–20. Cyclone Device Performance								
Resource Used	Design Size & Function	Mode	Resources Used			Performance		
			LEs	M4K Memory Bits	M4K Memory Blocks	-6 Speed Grade (MHz)	-7 Speed Grade (MHz)	-8 Speed Grade (MHz)
LE	16-to-1 multiplexer	-	21	-	-	405.00	320.00	275.00
	32-to-1 multiplexer	-	44	-	-	317.36	284.98	260.15
	16-bit counter	-	16	-	-	405.00	320.00	275.00
	64-bit counter (1)	-	66	-	-	208.99	181.98	160.75
M4K memory block	RAM 128 × 36 bit	Single port	-	4,608	1	256.00	222.67	197.01
	RAM 128 × 36 bit	Simple dual-port mode	-	4,608	1	255.95	222.67	196.97
	RAM 256 × 18 bit	True dual-port mode	-	4,608	1	255.95	222.67	196.97
	FIFO 128 × 36 bit	-	40	4,608	1	256.02	222.67	197.01
	Shift register 9 × 4 × 128	Shift register	11	4,536	1	255.95	222.67	196.97

Note to Table 4–20:

- (1) The performance numbers for this function are from an EP1C6 device in a 240-pin PQFP package.

Internal Timing Parameters

Internal timing parameters are specified on a speed grade basis independent of device density. **Tables 4–21** through **4–24** describe the Cyclone device internal timing microparameters for LEs, IOEs, M4K memory structures, and MultiTrack interconnects.

Table 4–21. LE Internal Timing Microparameter Descriptions (Part 1 of 2)	
Symbol	Parameter
t_{SU}	LE register setup time before clock
t_H	LE register hold time after clock

Table 4–21. LE Internal Timing Microparameter Descriptions (Part 2 of 2)

Symbol	Parameter
t_{CO}	LE register clock-to-output delay
t_{LUT}	LE combinatorial LUT delay for data-in to data-out
t_{CLR}	Minimum clear pulse width
t_{PRE}	Minimum preset pulse width
t_{CLKHL}	Minimum clock high or low time

Table 4–22. IOE Internal Timing Microparameter Descriptions

Symbol	Parameter
t_{SU}	IOE input and output register setup time before clock
t_H	IOE input and output register hold time after clock
t_{CO}	IOE input and output register clock-to-output delay
$t_{PIN2COMBOUT_R}$	Row input pin to IOE combinatorial output
$t_{PIN2COMBOUT_C}$	Column input pin to IOE combinatorial output
$t_{COMBIN2PIN_R}$	Row IOE data input to combinatorial output pin
$t_{COMBIN2PIN_C}$	Column IOE data input to combinatorial output pin
t_{CLR}	Minimum clear pulse width
t_{PRE}	Minimum preset pulse width
t_{CLKHL}	Minimum clock high or low time

Table 4–23. M4K Block Internal Timing Microparameter Descriptions

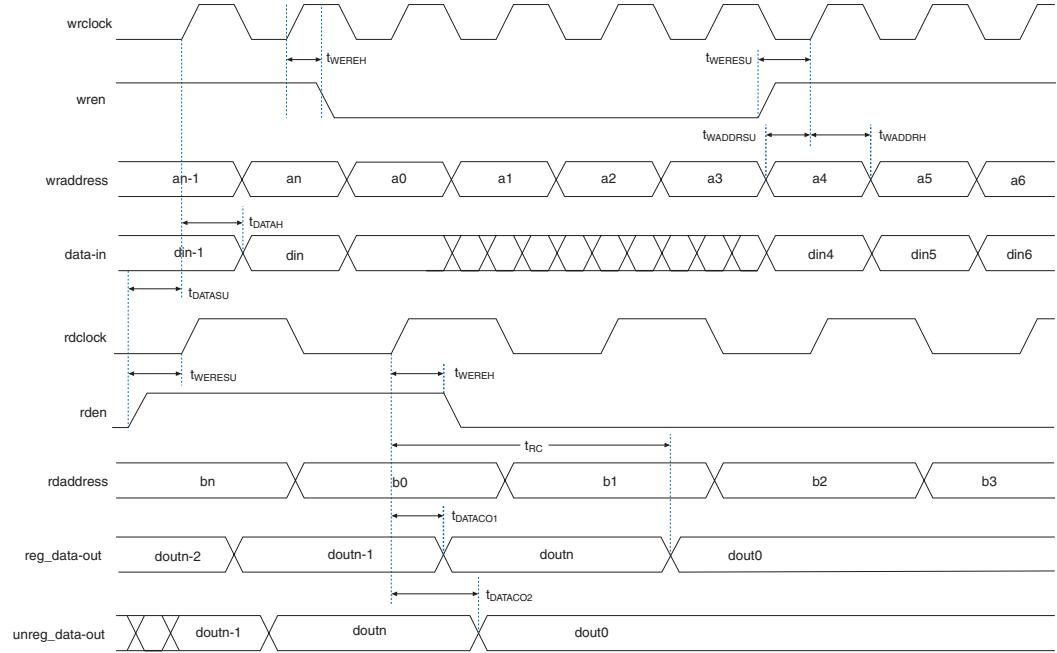
Symbol	Parameter
t_{M4KRC}	Synchronous read cycle time
t_{M4KWC}	Synchronous write cycle time
$t_{M4KWERESU}$	Write or read enable setup time before clock
$t_{M4KWEREH}$	Write or read enable hold time after clock
$t_{M4KBESU}$	Byte enable setup time before clock
t_{M4KBEH}	Byte enable hold time after clock
$t_{M4KDATABSU}$	A port data setup time before clock
$t_{M4KDATABAH}$	A port data hold time after clock
$t_{M4KADDRASU}$	A port address setup time before clock
$t_{M4KADDRAH}$	A port address hold time after clock
$t_{M4KDATABSU}$	B port data setup time before clock
$t_{M4KDATABH}$	B port data hold time after clock
$t_{M4KADDRBSU}$	B port address setup time before clock
$t_{M4KADDRBH}$	B port address hold time after clock
$t_{M4KDATACO1}$	Clock-to-output delay when using output registers
$t_{M4KDATAQ02}$	Clock-to-output delay without output registers
$t_{M4KCLKHL}$	Minimum clock high or low time
t_{M4KCLR}	Minimum clear pulse width

Table 4–24. Routing Delay Internal Timing Microparameter Descriptions

Symbol	Parameter
t_{R4}	Delay for an R4 line with average loading; covers a distance of four LAB columns
t_{C4}	Delay for an C4 line with average loading; covers a distance of four LAB rows
t_{LOCAL}	Local interconnect delay

Figure 4–1 shows the memory waveforms for the M4K timing parameters shown in Table 4–23.

Figure 4–1. Dual-Port RAM Timing Microparameter Waveform



Internal timing parameters are specified on a speed grade basis independent of device density. Tables 4–25 through 4–28 show the internal timing microparameters for LEs, IOEs, TriMatrix memory structures, DSP blocks, and MultiTrack interconnects.

Table 4–25. LE Internal Timing Microparameters (Part 1 of 2)

Symbol	-6		-7		-8		Unit
	Min	Max	Min	Max	Min	Max	
t_{SU}	29		33		37		ps
t_H	12		13		15		ps
t_{CO}		173		198		224	ps
t_{LUT}		454		522		590	ps

Table 4–25. LE Internal Timing Microparameters (Part 2 of 2)

Symbol	-6		-7		-8		Unit
	Min	Max	Min	Max	Min	Max	
t_{CLR}	129		148		167		ps
t_{PRE}	129		148		167		ps
t_{CLKHL}	107		123		139		ps

Table 4–26. IOE Internal Timing Microparameters

Symbol	-6		-7		-8		Unit
	Min	Max	Min	Max	Min	Max	
t_{SU}	348		400		452		ps
t_H	0		0		0		ps
t_{CO}		511		587		664	ps
$t_{PIN2COMBOUT_R}$		1,130		1,299		1,469	ps
$t_{PIN2COMBOUT_C}$		1,135		1,305		1,475	ps
$t_{COMBIN2PIN_R}$		2,627		3,021		3,415	ps
$t_{COMBIN2PIN_C}$		2,615		3,007		3,399	ps
t_{CLR}	280		322		364		ps
t_{PRE}	280		322		364		ps
t_{CLKHL}	95		109		123		ps

Table 4–27. M4K Block Internal Timing Microparameters (Part 1 of 2)

Symbol	-6		-7		-8		Unit
	Min	Max	Min	Max	Min	Max	
t_{M4KRC}		4,379		5,035		5,691	ps
t_{M4KWC}		2,910		3,346		3,783	ps
$t_{M4KWERESU}$	72		82		93		ps
$t_{M4KWEREH}$	43		49		55		ps
$t_{M4KBESU}$	72		82		93		ps
t_{M4KBEH}	43		49		55		ps
$t_{M4KDATAASU}$	72		82		93		ps
$t_{M4KDATAAH}$	43		49		55		ps

Table 4–27. M4K Block Internal Timing Microparameters (Part 2 of 2)

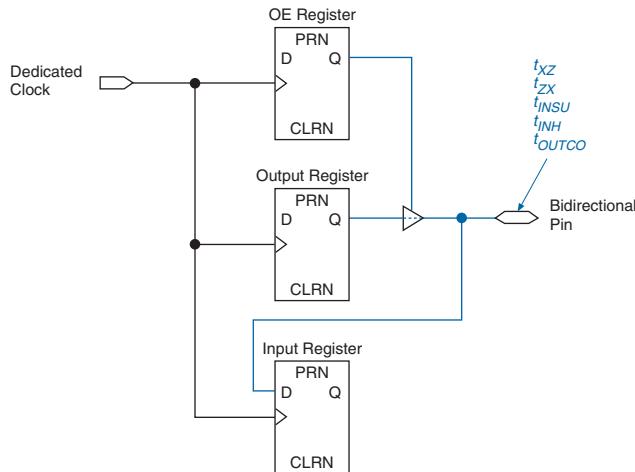
Symbol	-6		-7		-8		Unit
	Min	Max	Min	Max	Min	Max	
$t_{M4KADDRASU}$	72		82		93		ps
$t_{M4KADDRAH}$	43		49		55		ps
$t_{M4KDATABSU}$	72		82		93		ps
$t_{M4KDATABH}$	43		49		55		ps
$t_{M4KADDRBSU}$	72		82		93		ps
$t_{M4KADDRBH}$	43		49		55		ps
$t_{M4KDATACO1}$		621		714		807	ps
$t_{M4KDATACO2}$		4,351		5,003		5,656	ps
$t_{M4KCLKHL}$	105		120		136		ps
t_{M4KCLR}	286		328		371		ps

Table 4–28. Routing Delay Internal Timing Microparameters

Symbol	-6		-7		-8		Unit
	Min	Max	Min	Max	Min	Max	
t_{R4}		261		300		339	ps
t_{C4}		338		388		439	ps
t_{LOCAL}		244		281		318	ps

External Timing Parameters

External timing parameters are specified by device density and speed grade. [Figure 4–2](#) shows the timing model for bidirectional IOE pin timing. All registers are within the IOE.

Figure 4–2. External Timing in Cyclone Devices

All external I/O timing parameters shown are for 3.3-V LVTTL I/O standard with the maximum current strength and fast slew rate. For external I/O timing using standards other than LVTTL or for different current strengths, use the I/O standard input and output delay adders in Tables 4–40 through 4–44.

Table 4–29 shows the external I/O timing parameters when using global clock networks.

Table 4–29. Cyclone Global Clock External I/O Timing Parameters Notes (1), (2) (Part 1 of 2)

Symbol	Parameter	Conditions
t_{INSU}	Setup time for input or bidirectional pin using IOE input register with global clock fed by CLK pin	
t_{INH}	Hold time for input or bidirectional pin using IOE input register with global clock fed by CLK pin	
t_{OUTCO}	Clock-to-output delay output or bidirectional pin using IOE output register with global clock fed by CLK pin	$C_{LOAD} = 10 \text{ pF}$
t_{XZ}	Synchronous column IOE output enable register to output pin disable delay using global clock fed by CLK pin	$C_{LOAD} = 10 \text{ pF}$
t_{ZX}	Synchronous column IOE output enable register to output pin enable delay using global clock fed by CLK pin	$C_{LOAD} = 10 \text{ pF}$
$t_{INSUPLL}$	Setup time for input or bidirectional pin using IOE input register with global clock fed by Enhanced PLL with default phase setting	

Table 4–29. Cyclone Global Clock External I/O Timing Parameters		<i>Notes (1), (2) (Part 2 of 2)</i>
Symbol	Parameter	Conditions
t_{INHPLL}	Hold time for input or bidirectional pin using IOE input register with global clock fed by enhanced PLL with default phase setting	
$t_{OUTCOPLL}$	Clock-to-output delay output or bidirectional pin using IOE output register with global clock enhanced PLL with default phase setting	$C_{LOAD} = 10 \text{ pF}$
t_{XZPLL}	Synchronous column IOE output enable register to output pin disable delay using global clock fed by enhanced PLL with default phase setting	$C_{LOAD} = 10 \text{ pF}$
t_{ZXPLL}	Synchronous column IOE output enable register to output pin enable delay using global clock fed by enhanced PLL with default phase setting	$C_{LOAD} = 10 \text{ pF}$

Notes to Table 4–29:

- (1) These timing parameters are sample-tested only.
- (2) These timing parameters are for IOE pins using a 3.3-V LVTTL, 24-mA setting. Designers should use the Quartus II software to verify the external timing for any pin.

Tables 4–30 through 4–31 show the external timing parameters on column and row pins for EP1C3 devices.

Table 4–30. EP1C3 Column Pin Global Clock External I/O Timing Parameters							
Symbol	-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	3.085		3.547		4.009		ns
t_{INH}	0.000		0.000		0.000		ns
t_{OUTCO}	2.000	4.073	2.000	4.682	2.000	5.295	ns
t_{xz}		4.035		4.638		5.245	ns
t_{zx}		4.035		4.638		5.245	ns
$t_{INSUPLL}$	1.795		2.063		2.332		ns
t_{INHPLL}	0.000		0.000		0.000		ns
$t_{OUTCOPLL}$	0.500	2.306	0.500	2.651	0.500	2.998	ns
t_{XZPLL}		2.268		2.607		2.948	ns
t_{ZXPLL}		2.268		2.607		2.948	ns

Table 4–31. EP1C3 Row Pin Global Clock External I/O Timing Parameters

Symbol	-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	3.157		3.630		4.103		ns
t_{INH}	0.000		0.000		0.000		ns
t_{OUTCO}	2.000	3.984	2.000	4.580	2.000	5.180	ns
t_{xz}		3.905		4.489		5.077	ns
t_{zx}		3.905		4.489		5.077	ns
$t_{INSUPLL}$	1.867		2.146		2.426		ns
t_{INHPLL}	0.000		0.000		0.000		ns
$t_{OUTCOPLL}$	0.500	2.217	0.500	2.549	0.500	2.883	ns
t_{xzPLL}		2.138		2.458		2.780	ns
t_{zxPLL}		2.138		2.458		2.780	ns

Tables 4–32 through 4–33 show the external timing parameters on column and row pins for EP1C4 devices.

Table 4–32. EP1C4 Column Pin Global Clock External I/O Timing Parameters Note (1)

Symbol	-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.671		3.071		3.470		ns
t_{INH}	0.000		0.000		0.000		ns
t_{OUTCO}	2.000	3.937	2.000	4.526	2.000	5.119	ns
t_{xz}		3.899		4.482		5.069	ns
t_{zx}		3.899		4.482		5.069	ns
$t_{INSUPLL}$	1.471		1.690		1.910		ns
t_{INHPLL}	0.000		0.000		0.000		ns
$t_{OUTCOPLL}$	0.500	2.080	0.500	2.392	0.500	2.705	ns
t_{xzPLL}		2.042		2.348		2.655	ns
t_{zxPLL}		2.042		2.348		2.655	ns

Table 4–33. EP1C4 Row Pin Global Clock External I/O Timing Parameters Note (1)

Symbol	-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.800		3.220		3.639		ns
t_{INH}	0.000		0.000		0.000		ns
t_{OUTCO}	2.000	3.791	2.000	4.358	2.000	4.929	ns
t_{xz}		3.712		4.267		4.826	ns
t_{zx}		3.712		4.267		4.826	ns
$t_{INSUPLL}$	1.600		1.839		2.079		ns
t_{INHPLL}	0.000		0.000		0.000		ns
$t_{OUTCOPLL}$	0.500	1.934	0.500	2.224	0.500	2.515	ns
t_{xzPLL}		1.855		2.133		2.412	ns
t_{zxPLL}		1.855		2.133		2.412	ns

Note to Tables 4–32 and 4–33:

- (1) Contact Altera Applications for EP1C4 device timing parameters.

Tables 4–34 through 4–35 show the external timing parameters on column and row pins for EP1C6 devices.

Table 4–34. EP1C6 Column Pin Global Clock External I/O Timing Parameters

Symbol	-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.691		3.094		3.496		ns
t_{INH}	0.000		0.000		0.000		ns
t_{OUTCO}	2.000	3.917	2.000	4.503	2.000	5.093	ns
t_{xz}		3.879		4.459		5.043	ns
t_{zx}		3.879		4.459		5.043	ns
$t_{INSUPLL}$	1.513		1.739		1.964		ns
t_{INHPLL}	0.000		0.000		0.000		ns
$t_{OUTCOPLL}$	0.500	2.038	0.500	2.343	0.500	2.651	ns
t_{xzPLL}		2.000		2.299		2.601	ns
t_{zxPLL}		2.000		2.299		2.601	ns

Table 4–35. EP1C6 Row Pin Global Clock External I/O Timing Parameters

Symbol	-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.774		3.190		3.605		ns
t_{INH}	0.000		0.000		0.000		ns
t_{OUTCO}	2.000	3.817	2.000	4.388	2.000	4.963	ns
t_{xz}		3.738		4.297		4.860	ns
t_{zx}		3.738		4.297		4.860	ns
$t_{INSUPLL}$	1.596		1.835		2.073		ns
t_{INHPLL}	0.000		0.000		0.000		ns
$t_{OUTCOPLL}$	0.500	1.938	0.500	2.228	0.500	2.521	ns
t_{xzPLL}		1.859		2.137		2.418	ns
t_{zxPLL}		1.859		2.137		2.418	ns

Tables 4–36 through 4–37 show the external timing parameters on column and row pins for EP1C12 devices.

Table 4–36. EP1C12 Column Pin Global Clock External I/O Timing Parameters

Symbol	-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.510		2.885		3.259		ns
t_{INH}	0.000		0.000		0.000		ns
t_{OUTCO}	2.000	3.798	2.000	4.367	2.000	4.940	ns
t_{xz}		3.760		4.323		4.890	ns
t_{zx}		3.760		4.323		4.890	ns
$t_{INSUPLL}$	1.588		1.824		2.061		ns
t_{INHPLL}	0.000		0.000		0.000		ns
$t_{OUTCOPLL}$	0.500	1.663	0.500	1.913	0.500	2.164	ns
t_{xzPLL}		1.625		1.869		2.114	ns
t_{zxPLL}		1.625		1.869		2.114	ns

Table 4–37. EP1C12 Row Pin Global Clock External I/O Timing Parameters

Symbol	-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.620		3.012		3.404		ns
t_{INH}	0.000		0.000		0.000		ns
t_{OUTCO}	2.000	3.671	2.000	4.221	2.000	4.774	ns
t_{xz}		3.592		4.130		4.671	ns
t_{zx}		3.592		4.130		4.671	ns
$t_{INSUPLL}$	1.698		1.951		2.206		ns
t_{INHPLL}	0.000		0.000		0.000		ns
$t_{OUTCOPLL}$	0.500	1.536	0.500	1.767	0.500	1.998	ns
t_{xzPLL}		1.457		1.676		1.895	ns
t_{zxPLL}		1.457		1.676		1.895	ns

Tables 4–38 through 4–39 show the external timing parameters on column and row pins for EP1C20 devices.

Table 4–38. EP1C20 Column Pin Global Clock External I/O Timing Parameters

Symbol	-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.288		2.630		2.971		ns
t_{INH}	0.000		0.000		0.000		ns
t_{OUTCO}	2.000	3.870	2.000	4.450	2.000	5.033	ns
t_{xz}		3.832		4.406		4.983	ns
t_{zx}		3.832		4.406		4.983	ns
$t_{INSUPLL}$	1.288		1.480		1.671		ns
t_{INHPLL}	0.000		0.000		0.000		ns
$t_{OUTCOPLL}$	0.500	1.813	0.500	2.085	0.500	2.359	ns
t_{xzPLL}		1.775		2.041		2.309	ns
t_{zxPLL}		1.775		2.041		2.309	ns

Table 4–39. EP1C20 Row Pin Global Clock External I/O Timing Parameters

Symbol	-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.417		2.779		3.140		ns
t_{INH}	0.000		0.000		0.000		ns
t_{OUTCO}	2.000	3.724	2.000	4.282	2.000	4.843	ns
t_{xz}		3.645		4.191		4.740	ns
t_{zx}		3.645		4.191		4.740	ns
$t_{INSUPLL}$	1.417		1.629		1.840		ns
t_{INHPLL}	0.000		0.000		0.000		ns
$t_{OUTCOPLL}$	0.500	1.667	0.500	1.917	0.500	2.169	ns
t_{xzPLL}		1.588		1.826		2.066	ns
t_{zxPLL}		1.588		1.826		2.066	ns

External I/O Delay Parameters

External I/O delay timing parameters for I/O standard input and output adders and programmable input and output delays are specified by speed grade independent of device density.

Tables 4–40 through 4–45 show the adder delays associated with column and row I/O pins for all packages. If an I/O standard is selected other than LVTTL 24 mA with a fast slew rate, add the selected delay to the external t_{CO} and t_{SU} I/O parameters shown in Tables 4–25 through 4–28.

Table 4–40. Cyclone I/O Standard Column Pin Input Delay Adders (Part 1 of 2)

I/O Standard	-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
LVCMS		0		0		0	ps
3.3-V LVTTL		0		0		0	ps
2.5-V LVTTL		27		31		35	ps
1.8-V LVTTL		182		209		236	ps
1.5-V LVTTL		278		319		361	ps
SSTL-3 class I		-250		-288		-325	ps
SSTL-3 class II		-250		-288		-325	ps
SSTL-2 class I		-278		-320		-362	ps

Table 4–40. Cyclone I/O Standard Column Pin Input Delay Adders (Part 2 of 2)

I/O Standard	-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
SSTL-2 class II		-278		-320		-362	ps
LVDS		-261		-301		-340	ps

Table 4–41. Cyclone I/O Standard Row Pin Input Delay Adders

I/O Standard	-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
LVC MOS		0		0		0	ps
3.3-V LV TTL		0		0		0	ps
2.5-V LV TTL		27		31		35	ps
1.8-V LV TTL		182		209		236	ps
1.5-V LV TTL		278		319		361	ps
3.3-V PCI (1)		0		0		0	ps
SSTL-3 class I		-250		-288		-325	ps
SSTL-3 class II		-250		-288		-325	ps
SSTL-2 class I		-278		-320		-362	ps
SSTL-2 class II		-278		-320		-362	ps
LVDS		-261		-301		-340	ps

Table 4–42. Cyclone I/O Standard Output Delay Adders for Fast Slew Rate on Column Pins (Part 1 of 2)

Standard	-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit	
	Min	Max	Min	Max	Min	Max		
LVC MOS	2 mA		993		1,142		1,291	ps
	4 mA		504		579		655	ps
	8 mA		138		158		179	ps
	12 mA		0		0		0	ps
3.3-V LV TTL	4 mA		993		1,142		1,291	ps
	8 mA		646		742		839	ps
	12 mA		135		155		175	ps
	16 mA		174		200		226	ps
	24 mA		0		0		0	ps

Table 4–42. Cyclone I/O Standard Output Delay Adders for Fast Slew Rate on Column Pins (Part 2 of 2)

Standard		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	
2.5-V LVTTL	2 mA		1,322		1,520		1,718	ps
	8 mA		332		381		431	ps
	12 mA		338		388		439	ps
	16 mA		198		227		257	ps
1.8-V LVTTL	2 mA		997		1,146		1,296	ps
	8 mA		785		902		1,020	ps
	12 mA		785		902		1,020	ps
1.5-V LVTTL	2 mA		3,281		3,773		4,265	ps
	4 mA		1,601		1,841		2,081	ps
	8 mA		1,285		1,477		1,670	ps
SSTL-3 class I			583		670		758	ps
SSTL-3 class II			182		209		236	ps
SSTL-2 class I			508		584		660	ps
SSTL-2 class II			235		270		305	ps
LVDS			-5		-6		-7	ps

Table 4–43. Cyclone I/O Standard Output Delay Adders for Fast Slew Rate on Row Pins (Part 1 of 2)

Standard		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	
LVCMOS	2 mA		993		1,142		1,291	ps
	4 mA		504		579		655	ps
	8 mA		138		158		179	ps
	12 mA		0		0		0	ps
3.3-V LVTTL	4 mA		993		1,142		1,291	ps
	8 mA		646		742		839	ps
	12 mA		135		155		175	ps
	16 mA		174		200		226	ps
	24 mA		0		0		0	ps
2.5-V LVTTL	2 mA		1,322		1,520		1,718	ps
	8 mA		332		381		431	ps
	12 mA		338		388		439	ps
	16 mA		198		227		257	ps

Table 4–43. Cyclone I/O Standard Output Delay Adders for Fast Slew Rate on Row Pins (Part 2 of 2)

Standard		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	
1.8-V LVTTL	2 mA		2,283		2,625		2,968	ps
	8 mA		997		1,146		1,296	ps
	12 mA		785		902		1,020	ps
1.5-V LVTTL	2 mA		3,281		3,773		4,265	ps
	4 mA		1,601		1,841		2,081	ps
	8 mA		1,285		1,477		1,670	ps
3.3-V PCI (1)			116		133		150	ps
SSTL-3 class I			583		670		758	ps
SSTL-3 class II			182		209		236	ps
SSTL-2 class I			508		584		660	ps
SSTL-2 class II			235		270		305	ps
LVDS			-5		-6		-7	ps

Table 4–44. Cyclone I/O Standard Output Delay Adders for Slow Slew Rate on Column Pins (Part 1 of 2)

I/O Standard		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	
LVCMOS	2 mA		2,793		3,212		3,631	ps
	4 mA		2,304		2,649		2,995	ps
	8 mA		1,938		2,228		2,519	ps
	12 mA		1,800		2,070		2,340	ps
3.3-V LVTTL	4 mA		2,824		3,247		3,671	ps
	8 mA		2,477		2,847		3,219	ps
	12 mA		1,966		2,260		2,555	ps
	16 mA		2,005		2,305		2,606	ps
	24 mA		1,831		2,105		2,380	ps
2.5-V LVTTL	2 mA		3,740		4,300		4,861	ps
	8 mA		2,750		3,161		3,574	ps
	12 mA		2,756		3,168		3,582	ps
	16 mA		2,616		3,007		3,400	ps
1.8-V LVTTL	2 mA		6,499		7,473		8,448	ps
	8 mA		5,213		5,994		6,776	ps
	12 mA		5,001		5,750		6,500	ps

Table 4–44. Cyclone I/O Standard Output Delay Adders for Slow Slew Rate on Column Pins (Part 2 of 2)

I/O Standard		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	
1.5-V LVTTL	2 mA		7,782		8,949		10,116	ps
	4 mA		6,102		7,017		7,932	ps
	8 mA		5,786		6,653		7,521	ps
SSTL-3 class I			2,383		2,740		3,098	ps
SSTL-3 class II			1,982		2,279		2,576	ps
SSTL-2 class I			2,958		3,401		3,845	ps
SSTL-2 class II			2,685		3,087		3,490	ps
LVDS			1,795		2,064		2,333	ps

Table 4–45. Cyclone I/O Standard Output Delay Adders for Slow Slew Rate on Row Pins (Part 1 of 2)

I/O Standard		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	
LVCMOS	2 mA		2,793		3,212		3,631	ps
	4 mA		2,304		2,649		2,995	ps
	8 mA		1,938		2,228		2,519	ps
	12 mA		1,800		2,070		2,340	ps
3.3-V LVTTL	4 mA		2,824		3,247		3,671	ps
	8 mA		2,477		2,847		3,219	ps
	12 mA		1,966		2,260		2,555	ps
	16 mA		2,005		2,305		2,606	ps
	24 mA		1,831		2,105		2,380	ps
2.5-V LVTTL	2 mA		3,740		4,300		4,861	ps
	8 mA		2,750		3,161		3,574	ps
	12 mA		2,756		3,168		3,582	ps
	16 mA		2,616		3,007		3,400	ps
1.8-V LVTTL	2 mA		6,499		7,473		8,448	ps
	8 mA		5,213		5,994		6,776	ps
	12 mA		5,001		5,750		6,500	ps
1.5-V LVTTL	2 mA		7,782		8,949		10,116	ps
	4 mA		6,102		7,017		7,932	ps
	8 mA		5,786		6,653		7,521	ps
3.3-V PCI			1,916		2,203		2,490	ps

Table 4–45. Cyclone I/O Standard Output Delay Adders for Slow Slew Rate on Row Pins (Part 2 of 2)

I/O Standard	-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
SSTL-3 class I		2,383		2,740		3,098	ps
SSTL-3 class II		1,982		2,279		2,576	ps
SSTL-2 class I		2,958		3,401		3,845	ps
SSTL-2 class II		2,685		3,087		3,490	ps
LVDS		1,795		2,064		2,333	ps

Note to Tables 4–40 through 4–45:

(1) EP1C3 devices do not support the PCI I/O standard.

Tables 4–46 through 4–47 show the adder delays for the IOE programmable delays. These delays are controlled with the Quartus II software options listed in the Parameter column.

Table 4–46. Cyclone IOE Programmable Delays on Column Pins

Parameter	Setting	-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	
Decrease input delay to internal cells	Off		3,057		3,515		3,974	ps
	Small		2,639		3,034		3,430	ps
	Medium		2,212		2,543		2,875	ps
	Large		155		178		201	ps
	On		155		178		201	ps
Decrease input delay to input register	Off		3,057		3,515		3,974	ps
	On		0		0		0	ps
Increase delay to output pin	Off		0		0		0	ps
	On		552		634		717	ps

Table 4–47. Cyclone IOE Programmable Delays on Row Pins

Parameter	Setting	-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	
Decrease input delay to internal cells	Off		3,057		3,515		3,974	ps
	Small		2,639		3,034		3,430	ps
	Medium		2,212		2,543		2,875	ps
	Large		154		177		200	ps
	On		154		177		200	ps
Decrease input delay to input register	Off		3,057		3,515		3,974	ps
	On		0		0		0	ps
Increase delay to output pin	Off		0		0		0	ps
	On		556		639		722	ps

Maximum Input & Output Clock Rates

Tables 4–48 and 4–49 show the maximum input clock rate for column and row pins in Cyclone devices.

Table 4–48. Cyclone Maximum Input Clock Rate for Column Pins

I/O Standard	-6 Speed Grade	-7 Speed Grade	-8 Speed Grade	Unit
LVTTL	464	428	387	MHz
2.5 V	392	302	207	MHz
1.8 V	387	311	252	MHz
1.5 V	387	320	243	MHz
LVCMOS	405	374	333	MHz
SSTL-3 class I	405	356	293	MHz
SSTL-3 class II	414	365	302	MHz
SSTL-2 class I	464	428	396	MHz
SSTL-2 class II	473	432	396	MHz
LVDS	567	549	531	MHz

Table 4–49. Cyclone Maximum Input Clock Rate for Row Pins

I/O Standard	-6 Speed Grade	-7 Speed Grade	-8 Speed Grade	Unit
LVTTL	464	428	387	MHz
2.5 V	392	302	207	MHz
1.8 V	387	311	252	MHz
1.5 V	387	320	243	MHz
LVCMOS	405	374	333	MHz
SSTL-3 class I	405	356	293	MHz
SSTL-3 class II	414	365	302	MHz
SSTL-2 class I	464	428	396	MHz
SSTL-2 class II	473	432	396	MHz
3.3-V PCI (1)	464	428	387	MHz
LVDS	567	549	531	MHz

Note to [Tables 4–48 through 4–49](#):

- (1) EP1C3 devices do not support the PCI I/O standard. These parameters are only available on row I/O pins.

[Tables 4–50](#) and [4–51](#) show the maximum output clock rate for column and row pins in Cyclone devices.

Table 4–50. Cyclone Maximum Output Clock Rate for Column Pins

I/O Standard	-6 Speed Grade	-7 Speed Grade	-8 Speed Grade	Unit
LVTTL	296	285	273	MHz
2.5 V	381	366	349	MHz
1.8 V	286	277	267	MHz
1.5 V	219	208	195	MHz
LVCMOS	367	356	343	MHz
SSTL-3 class I	169	166	162	MHz
SSTL-3 class II	160	151	146	MHz
SSTL-2 class I	160	151	142	MHz
SSTL-2 class II	131	123	115	MHz
LVDS	328	303	275	MHz

Table 4–51. Cyclone Maximum Output Clock Rate for Row Pins

I/O Standard	-6 Speed Grade	-7 Speed Grade	-8 Speed Grade	Unit
LVTTL	296	285	273	MHz
2.5 V	381	366	349	MHz
1.8 V	286	277	267	MHz
1.5 V	219	208	195	MHz
LVCMOS	367	356	343	MHz
SSTL-3 class I	169	166	162	MHz
SSTL-3 class II	160	151	146	MHz
SSTL-2 class I	160	151	142	MHz
SSTL-2 class II	131	123	115	MHz
3.3-V PCI (1)	66	66	66	MHz
LVDS	328	303	275	MHz

Note to Tables 4–50 through 4–51:

- (1) EP1C3 devices do not support the PCI I/O standard. These parameters are only available on row I/O pins.

PLL Timing

Table 4–52 describes the Cyclone FPGA PLL specifications.

Table 4–52. Cyclone PLL Specifications Note (1) (Part 1 of 2)

Symbol	Parameter	Min	Max	Unit
f_{IN}	Input frequency (-6 speed grade)	15.625	464	MHz
	Input frequency (-7 speed grade)	15.625	428	MHz
	Input frequency (-8 speed grade)	15.625	387	MHz
$f_{IN\ DUTY}$	Input clock duty cycle	40.00	60	%
$t_{IN\ JITTER}$	Input clock period jitter		± 200	ps
f_{OUT_EXT} (external PLL clock output)	PLL output frequency (-6 speed grade)	15.625	320	MHz
	PLL output frequency (-7 speed grade)	15.625	320	MHz
	PLL output frequency (-8 speed grade)	15.625	275	MHz

Table 4–52. Cyclone PLL Specifications		<i>Note (1) (Part 2 of 2)</i>		
Symbol	Parameter	Min	Max	Unit
f_{OUT} (to global clock)	PLL output frequency (-6 speed grade)	15.625	405	MHz
	PLL output frequency (-7 speed grade)	15.625	320	MHz
	PLL output frequency (-8 speed grade)	15.625	275	MHz
$t_{\text{OUT DUTY}}$	Duty cycle for external clock output (when set to 50%)	45.00	55	%
$t_{\text{JITTER}} \text{ (2)}$	Period jitter for external clock output		$\pm 300 \text{ (3)}$	ps
$t_{\text{LOCK}} \text{ (4)}$	Time required to lock from end of device configuration	10.00	100	μs
f_{VCO}	PLL internal VCO operating range	500.00	1,000	MHz
M	Counter values	2 to 32		integer
N, G0, G1, E	Counter values	1	32	integer

Notes to Table 4–52:

- (1) These numbers are preliminary and pending silicon characterization.
- (2) The t_{JITTER} specification for the $\text{PLL}[2..1]_{\text{OUT}}$ pins are dependent on the I/O pins in its V_{CCIO} bank, how many of them are switching outputs, how much they toggle, and whether or not they use programmable current strength or slow slew rate.
- (3) $f_{\text{OUT}} \geq 100 \text{ MHz}$. When the PLL external clock output frequency (f_{OUT}) is smaller than 100 MHz, the jitter specification is 60 mUI.
- (4) $f_{\text{IN/N}}$ must be greater than 200 MHz to ensure correct lock circuit operation below -20°C .